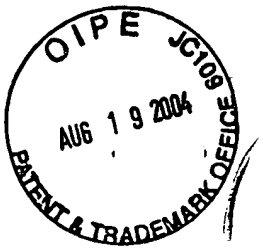

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Whitman et al.

Serial No.: 09/997,019

Filed: November 28, 2001

For: SPIN COATING FOR MAXIMUM FILL CHARACTERISTIC YIELDING A PLANARIZED THIN FILM SURFACE

Confirmation No.: 6139

Examiner: B. Kebede

Group Art Unit: 2823

Attorney Docket No.: 2269-4294.2US

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APPEAL BRIEF

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Attn: Board of Patent Appeals and Interferences

Sirs:

This Appeal Brief is being submitted in triplicate and in the format of 37 C.F.R. § 1.192(c). A check in the amount of $330.00 for the fee under 37 C.F.R § 1.17(c) for filing a brief in support of an appeal is enclosed.

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(1) REAL PARTY IN INTEREST

The real party in interest in the above-referenced appeal is Micron Technology, Inc., the assignee of the above-referenced application as recorded with the United States Patent and Trademark Office on April 4, 2000, Reel 010729, Frame 0057.

(2) RELATED APPEALS AND INTERFERENCES

The Examiner's rejections in the parent of the above-referenced application, U.S. Patent application serial no. 09/542,783, filed April 4, 2000 (hereinafter "the '783 Application"), are currently the subject of an appeal, as are the Examiner's rejections in a related application, U.S. Patent application serial no. 09/996,423, filed November 28, 2001.

(3) STATUS OF THE CLAIMS

Claims 1-22 are currently pending and under consideration in the above-referenced application.

Each of claims 1-22 stands rejected.

The rejections of claims 1-22 are being appealed.

(4) STATUS OF AMENDMENTS

The above-referenced application, U.S. Patent application serial no. 09/997,019 (hereinafter "the '019 Application"), was filed on November 28, 2001, as a divisional of the '783 Application. The '019 Application was originally filed with 22 claims.

A Preliminary Amendment was mailed on February 12, 2002, to correct grammatical and formal errors in the claims.

A first Office Action on the merits was mailed by the Office on February 20, 2003. Each of claims 1-22 was rejected.

A response to the first Office Action was filed on May 23, 2003. That response included explanations of the patentability of claims 1-22.

As evidenced by a second, non-final Office Action dated August 29, 2003, the Examiner was convinced by Appellants' arguments and presented new grounds for rejecting claims 1-22

Thereafter, on December 1, 2003, an Amendment was filed. The Amendment of December 1, 2003, included minor claim revisions, in which some occurrences of the term "said" were removed and the remaining occurrences of the term "said" were replaced with the equivalent term "the." In addition, the Amendment included an analysis of the art that had been relied upon in rejecting claims 1-22, highlighting the patentability of the claims over the art.

A Final Office Action followed on February 19, 2004. In the Final Office Action, the rejections of claims 1-22 were maintained.

In an Amendment Under 37 C.F.R. § 1.116, which was filed on April 23, 2004, independent claim 1 was amended to remove the term "substantially," thus narrowing the number of issues that remained for purposes of this Appeal. In addition, further remarks were presented to establish the patentability of claims 1-22 over the art upon which the rejections of these claims were based.

In an Advisory Action dated May 10, 2004, the Office indicated that the Examiner was not convinced by the explanations that had been provided by Appellants, but that the proposed

claim amendment would be entered upon appeal of the Examiner's rejections in the above-referenced application.

A Notice of Appeal was promptly filed on May 19, 2004.

This Appeal Brief is being filed by August 19, 2004, with a petition and the appropriate fee for a one-month extension of the two-month shortened statutory period for filing an Appeal Brief following the filing of a Notice of Appeal.

(5) SUMMARY OF THE INVENTION

The claims that have been considered in the above-referenced application are drawn to methods for preparing the surface of semiconductor device structures for planarization.

In the inventive methods, a semiconductor device structure is provided. *See, e.g.,* Paragraphs **[0012]**, **[0045]**, **[0046]**, **[0052]**, **[0053]**, Figs. 7 and 12. The semiconductor device structure includes at least one recess in a surface thereof. *Id.* A first material layer substantially fills the recess and covers the surface. *Id.* A second material is then applied to the first material layer. *Id.* The second material is spread over the first material layer. *Id.* The resulting second material layer has a planar surface and does not require further planarization. *Id.*

(6) ISSUES

(A) Whether claims 1, 2, 6, 7, and 10-22 recite subject matter which is novel over the subject matter described in U.S. Patent 6,461,932 to Wang (hereinafter "Wang");

(B) Whether, under 35 U.S.C. § 103(a), claims 3-5 are allowable for being drawn to subject matter which is patentable over the teachings of Wang, in view of teachings from U.S. Patent 6,117,486 to Yoshihara (hereinafter "Yoshihara"); and

(C) Whether claims 8 and 9 recite subject matter which, under 35 U.S.C. § 103(a), is patentable over teachings from Wang and U.S. Patent 6,228,711 to Hsieh (hereinafter "Hsieh").

(7) GROUPING OF CLAIMS

Group 1 – Claims 1, 2, 6, 7, and 10-22:

For purposes of the 35 U.S.C. § 102 rejections, claims 1, 2, 6, 7, and 10-22 should be grouped together. Claim 1 is the most generic claim of this group. Claims 2, 6, 7, and 10-22 stand with claim 1 but, for the reasons set forth in the ARGUMENT section of this Appeal Brief, none of claims 2, 10, 13, or 15 falls with claim 1.

Group 2 – Claims 3-5:

For purposes of the 35 U.S.C. § 103(a) that has been based on the teachings of Wang and Yoshihara, claims 3-5 should be grouped together. Claim 3 is the most generic claim of this group. Claims 4 and 5 stand and fall with claim 3.

Group 3 – Claims 8 and 9:

With respect to the 35 U.S.C. § 103(a) rejection that has been based on teachings from Wang and Hsieh, claims 8 and 9 should be grouped together. Claim 8 is the most generic claim of this group. Claim 9 stands and falls with claim 8.

(8) ARGUMENT

(A) REJECTIONS UNDER 35 U.S.C. § 102(e)

Claims 1, 2, 6, 7, and 10-22 stand rejected under 35 U.S.C. § 102(e) for reciting subject matter which is purportedly anticipated by the subject matter disclosed in Wang.

(1) RELEVANT LAW

A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single reference which qualifies as prior art under 35 U.S.C. § 102. *Verdegaal Brothers v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). The identical invention must be shown in as complete detail as is contained in the claim. *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

M.P.E.P. § 2125 provides that "[d]rawings and pictures can anticipate claims is they clearly show the structure which is claimed," but cautions that the "drawings must be evaluated for what they reasonably disclose and suggest to one of ordinary skill in the art." This rule is based, at least in part, upon the holding in *In re Aslanian,* 200 USPQ 500 (C.C.P.A. 1979), in which the court directed "[w]e evaluate and apply the teachings of all relevant references on the basis of what they reasonably disclose and suggested to one skilled in the art . . ." In *Aslanian,* the court was evaluating the relevance of drawings of a design patent as prior art to the claims of a patent application. Relative dimensions were not at issue, indicating that the guidance provided by M.P.E.P. § 2125 merely discusses relative dimensions of features of an illustrated object as an

example of something that may not be reasonably disclosed or suggested to one of ordinary skill in the art.

M.P.E.P. § 2125 also requires that arguments about illustrated drawing features, such as proportions and dimensions (*e.g.,* planarity or nonplanarity), are of little value when the specification does not indicate that the drawings may be relied upon for such a purpose. Neither the M.P.E.P. nor the relevant case law indicates, however, that an omission means that the subject matter illustrated in drawings must be taken at face value.

(2) REFERENCE RELIED UPON

Wang describes a process for creating a trench-isolated semiconductor structure "using a pre-smoothing technique to avoid difficulties such as dishing and premature silicon-nitride removal that might otherwise occur during chemical-mechanical polishing..." (hereinafter "CMP"). Col. 4, lines 48-51. While the avoidance of dishing a premature silicon nitride removal my prevent some of the nonplanarities that might occur during CMP, other types of nonplanarities may remain.

The process of Wang includes providing a dielectric layer 56 over a semiconductor surface, and covering the dielectric layer 56 with a "smoothening layer" 60. Col. 6, lines 23-28. The smoothening layer 60 has an upper smoothening surface 62 which is smoother than the upper dielectric surface 58 of the dielectric layer 56. Col. 6, lines 29-31. The smoothening layer 60 is applied either by a "deposition/spinning procedure" (col. 6, line 52, to col.7, line 14), a "deposition/flow" procedure (col. 7, lines 15-27), or a combination of these procedures (col. 7, lines 28-41).

Once the smoothening layer 60 has been formed, the smoothening layer 60 and the dielectric layer 56 are removed by CMP methods until a portion of the underlying semiconductor device is exposed. Col. 7, line 42, to col. 8, line 25.

(3) ANALYSIS

Fig. 4d of Wang illustrates the upper smoothening surface 62 of the smoothening layer 60 as being planar. The specification of Wang, however, does not disclose that the drawings may be relied upon at face value. It has been asserted, at page 9 of the Final Office Action, that an omission in the specification as to the reliability of the drawings means that the subject matter illustrated in drawings must be taken at face value. Again, M.P.E.P. § 2125 indicates that the features that are illustrated in drawings, such as proportions and dimensions (*e.g.*, planarity or nonplanarity), are of little value when the specification does not state that the drawings may be relied upon for such a purpose. Thus, according to M.P.E.P. § 2125, the drawings of Wang, specifically Fig. 4d, cannot be relied upon as disclosing that the upper smoothening surface 62 is substantially planar.

Moreover, when Fig. 4d is viewed in connection with the description of Wang, it is clear that Fig. 4d cannot be relied upon as showing a smoothening layer 60 with a planar upper smoothening surface 62. Instead, the description of Wang is limited to an upper smoothening surface 62 that is merely "largely planar." Wang even goes so far as to note that the term "largely planar" is a relative term and, thus, is merely used for the purpose of comparing the planarity of the upper smoothening surface 62 to the underlying and highly nonplanar upper dielectric surface 58. Col. 6, lines 35-36. Further, Wang clearly explains that "slight depressions [are

present] in upper smoothening surface 62 at locations of the deepest parts of the depressed portion of upper dielectric surface 58." Col. 6, lines 32-37.

(a) Claim 1

Independent claim 1 is directed to a method for preparing a surface of a semiconductor device structure for planarization. The method of amended independent claim 1 includes, among other things, spreading a second material over a first material layer having a nonplanar surface so as to form a second material layer having a planar surface.

Wang lacks any express or inherent description of spreading a second material layer over a first material layer so as to form a second material layer having a planar surface, as recited in independent claim 1. Instead, Wang describes a smoothening layer 60 that may include "slight depressions" in the upper smoothening surface 62 thereof. Col. 6, lines 32-34.

Accordingly, it is respectfully submitted that Wang does not anticipate each and every element of independent claim 1, as would be required to maintain the 35 U.S.C. § 102(e) rejection of independent claim 1. It is, therefore, respectfully submitted that, under 35 U.S.C. § 102(e), independent claim 1 recites subject matter which is allowable over that described in Wang.

It is also respectfully submitted that claims 2, 6, 7, and 10-22 are each allowable, among other reasons, for depending either directly or indirectly from claim 1, which is allowable.

(b) Claim 2

Claim 2 is additionally allowable because Wang lacks any express or inherent description that the smoothing layer 60 thereof comprises a stress buffer material. As explained at paragraph **[0018]** of the specification of the above-referenced application, a stress buffer material may "facilitate[] planarization . . . without causing substantial defects" in an underlying material layer. Wang lacks any express or inherent description that the smoothing layer 60 thereof facilitates planarization. Rather, the description of Wang is limited to a disclosure that the smoothing layer 60 prevents the formation of depressions in trench dielectric regions ("dishing") and/or the undesired removal of material underlying the dielectric material in the semiconductor structure, such as nitride or oxide layers, during CMP. Col. 2, lines 9-27.

Therefore, claim 2 recites subject matter which, under 35 U.S.C. 102(e), is allowable of the subject matter described in Wang.

(c) Claim 10

Claim 10, which depends from claim 2, is further allowable since Wang does not expressly or inherently describe that the smoothening layer 60 may be spread such that one valley of the underlying dielectric layer 56 may be at least partially filled while at least one peak of the underlying dielectric layer 56 may remain substantially uncovered. Instead, the description of Wang is quite clearly limited to applying the smoothening layer 60 in such a manner that "the depressed portion[s] of upper dielectric surface 58 above trench[es] 54" are completely filled. Col. 6, lines 26-27; Fig. 4d. None of the peaks of the dielectric layer 56 is exposed until after the CMP process has begun. *See* col. 7, line 65, to col. 8, line 4.

It is, therefore, respectfully submitted that, under 35 U.S.C. § 102(e), the subject matter to which claim 10 is directed is allowable over the subject matter described in Wang.

(d) Claim 13

Claim 13, which depends from claims 2, 10, 11, and 12, is additionally allowable since Wang includes no express or inherent description that the dielectric layer 56 may be *etched* with selectivity over the smoothening layer 60 thereof until a surface of at least one region of the dielectric layer 56 is in substantially the same plane as a surface of the smoothening layer 60. Instead, the dielectric layer 56 of Wang is not removed until after CMP of the smoothening layer 60 exposes it through the smoothening layer 60. Even then, it is through removal of the smoothening layer 60 by CMP that surfaces of the smoothening layer 60 and the dielectric layer 56 are made substantially coplanar. *See* col. 7, line 65, to col. 8, line 4; Fig. 4e.

Accordingly, it is respectfully submitted that the subject matter recited in claim 13 is not anticipated under 35 U.S.C. § 102(e) by the subject matter described in Wang and, thus, is allowable over the subject matter described in Wang.

(e) Claim 15

Claim 15, which depends from claims 2, 10, 11, 12, and 13, is additionally allowable since Wang includes no express or inherent description that the dielectric layer 56 and the smoothening layer 60 may be etched at substantially the same rate so as to expose a surface of the mask layer 44 adjacent a surface of a portion of the dielectric layer 56 in at least one recess, with the surfaces of the mask layer 44 and the dielectric layer 56 being located in substantially the

same plane following such planarization. Rather than describing etching processes to remove both the smoothening layer 60 and the dielectric layer 56, the description of Wang is limited to use of CMP.

It is, therefore, respectfully submitted that, under 35 U.S.C. § 102(e), claim 15 is drawn to subject matter which is allowable over the subject matter described in Wang.

In view of the foregoing, it is respectfully requested that the 35 U.S.C. § 102(e) rejections of claims 1, 2, 6, 7, and 10-22 be reversed.

(B) REJECTIONS UNDER 35 U.S.C. § 103(a)

Claims 3, 4, 5, 8, and 9 stand rejected under 35 U.S.C. § 103(a).

(1) RELEVANT LAW

The standard for establishing and maintaining a rejection under 35 U.S.C. § 103(a) is set forth in M.P.E.P. § 706.02(j), which provides:

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

(2) WANG AND YOSHIHARA – CLAIMS 3-5

Claims 3-5 have been rejected under 35 U.S.C. § 103(a) for being directed to subject matter which is allegedly unpatentable over the subject matter taught in Wang, in view of teachings from Yoshihara.

(a) ADDITIONAL REFERENCE RELIED UPON

Yoshihara teaches a method for forming photoresist layers that have a "predetermined" "uniform thickness" without any "ripples" therein. *See, e.g.,* Col. 2, line 33; col. 11, lines 48-54, 62; Fig. 9.

(b) ANALYSIS

Claims 3-5 are each allowable, among other reasons, for depending either directly or indirectly from claim 1, which is allowable.

Moreover, it is respectfully submitted that the Office has not established a *prima facie* case of obviousness against any of claims 3-5, as would be required to maintain the 35 U.S.C. § 103(a) rejections of these claims.

It is respectfully submitted that one of ordinary skill in the art would not have been motivated to combine the teachings of Wang with those of Yoshihara. Since Yoshihara teaches a process for forming a layer of uniform thickness, iif the process taught in Yoshihara were used to form the smoothening layer 60 of Wang, the smoothening layer 60 would have a uniform thickness. As a result, the smoothening surface 62 of the smoothening layer 60 would be as nonplanar as the upper surface of the underlying dielectric layer 56. *See* Wang, Fig. 4d.

Since the only expected result of the asserted combination of teachings would differ from the subject matter recited in independent claim 1, from which claims 3-5 depend, it appears that any motivation to combine the teachings of Yoshihara and Wang in the asserted manner could only have been improperly gleaned from the subject matter described in the '019 Application.

It is also respectfully submitted that a person of ordinary skill in the art at the time of the invention would have no reason to believe that combining the teachings of Wang and Yoshihara in the manner that has been asserted would have been successful. Again, use of the spin-on process taught in Yoshihara to form the smoothening layer 60 of Wang would have merely resulted in a structure with a smoothening layer 60 of substantially uniform thickness. Due to the substantially uniform thickness of the resulting smoothening layer 60, the upper smoothening surface 62 thereof would take on substantially the same topography as the uneven upper surface of the underlying dielectric layer 56. Thus, one of ordinary skill in the art would have no reason to expect the asserted combination of teachings from Wang and Yoshihara to result in a smoothening layer 60 that has a planar upper smoothening surface 62, as would be required to render the subject matter recited in independent claim 1, from which claims 3-5 depend, obvious and, thus, unpatentable.

For these reasons, it is respectfully submitted that, under 35 U.S.C. § 103(a) each of claims 3-5 is allowable over Wang and Yoshihara, taken either individually or together.

(3) WANG AND HSIEH – CLAIMS 8 & 9

Claims 8 and 9 stand rejected under 35 U.S.C. § 103(a) for reciting subject matter which is assertedly unpatentable over the teachings of Wang, in view of teachings from Hsieh.

Claims 8 and 9 are both allowable, among other reasons, as respectively depending directly and indirectly from claim 1, which is allowable.

In view of the foregoing, reversal of the 35 U.S.C. § 103(a) rejections of claims 3-5, 8, and 9 is respectfully requested.

(9) APPENDIX

A listing of claims 1-22 is included as an Appendix to this Appeal Brief.

(10) CONCLUSIONS

It is respectfully submitted that:

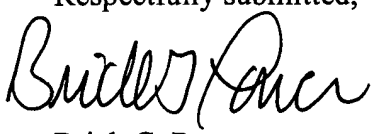
(A) Claims 1, 2, 6, 7, and 10-22 recite subject matter which is novel over the subject matter described in Wang;

(B) Claims 3-5 are allowable under 35 U.S.C. § 103(a) for being drawn to subject matter which is patentable over the teachings of Wang, in view of teachings from Yoshihara; and

(C) Claims 8 and 9 recite subject matter which, under 35 U.S.C. § 103(a), is patentable over teachings from Wang and Hsieh.

In view of the foregoing, it is respectfully requested that the Examiner's rejections of claims 1-22 be reversed and that each of these claims be allowed.

Respectfully submitted,



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APPENDIX

CLAIMS

1. (Previously presented) A method for preparing a surface of a semiconductor device structure for planarization, comprising:

providing a semiconductor device structure including at least one recess formed in a surface thereof and a first material layer substantially filling the at least one recess and covering the surface, the first material layer having a nonplanar surface;

applying a second material to the first material layer; and

spreading the second material over the first material layer so as to form a second material layer having a planar surface without requiring subsequent planarization of the second material.

2. (Previously presented) The method of claim 1, wherein applying the second material comprises applying a stress buffer material to the first material layer.

3. (Previously presented) The method of claim 1, wherein the spreading comprises:

spinning the semiconductor device structure at a first speed;

gradually decreasing a rate of the spinning to a second speed; and

gradually increasing a rate of the spinning to a third speed.

4. (Previously presented) The method of claim 3, wherein spinning the semiconductor device structure at the second speed comprises permitting the second material within the at least one recess to at least partially set.

5. (Previously presented) The method of claim 3, wherein spinning the semiconductor device structure at the third speed comprises forming the second material over the surface to a desired thickness.

6. (Previously presented) The method of claim 1, wherein providing comprises providing a shallow trench isolation structure with the at least one recess comprising at least one trench formed in a surface of the shallow trench isolation structure.

7. (Previously presented) The method of claim 6, wherein providing further comprises providing the shallow trench isolation structure with the first material layer comprising an electrical insulator material.

8. (Previously presented) The method of claim 1, wherein providing comprises providing a semiconductor device structure with the at least one recess comprising at least one dual damascene trench formed therein.

9. (Previously presented) The method of claim 8, wherein providing further comprises providing a semiconductor device structure with the first material layer comprising conductive material.

10. (Previously presented) The method of claim 2, wherein spreading comprises at least partially filling at least one valley of the first material layer with the stress buffer material while leaving at least one peak of the first material layer substantially uncovered by the stress buffer material.

11. (Previously presented) The method of claim 10, further comprising planarizing at least the first material layer.

12. (Previously presented) The method of claim 11, wherein planarizing comprises etching at least one region of the first material layer exposed through the stress buffer material with selectivity over the stress buffer material.

13. (Previously presented) The method of claim 12, wherein etching is effected until a surface of the at least one region is in substantially the same plane as a surface of the stress buffer material.

14. (Previously presented) The method of claim 13, wherein planarizing further comprises abrasively planarizing the stress buffer material and the at least one region to expose the surface of the semiconductor device structure adjacent the at least one recess, the surface of the semiconductor device structure and a surface of the first material layer in the at least one recess being located in substantially the same plane following planarizing.

15. (Previously presented) The method of claim 13, wherein planarizing further comprises concurrently etching the first material layer and the stress buffer material at substantially the same rate so as to expose the surface of the semiconductor device structure adjacent the at least one recess with the surface of the semiconductor device structure and a surface of the first material layer in the at least one recess being located in substantially the same plane following the planarizing.

16. (Previously presented) The method of claim 11, wherein planarizing is effected until the surface of the semiconductor device structure is exposed through the first material layer.

17. (Previously presented) The method of claim 16, wherein etching is effected until a surface of the first material layer in the at least one recess is in substantially the same plane as the surface of the semiconductor device structure.

18. (Previously presented) The method of claim 16, further comprising removing the stress buffer material from the semiconductor device structure.

19. (Previously presented) The method of claim 2, wherein spreading comprises forming a substantially planar surface over the semiconductor device structure.

20. (Previously presented) The method of claim 19, further comprising planarizing at least the first material layer.

21. (Previously presented) The method of claim 20, wherein planarizing comprises substantially concurrently abrasively planarizing the stress buffer material and the first material layer to expose the surface of the semiconductor device structure adjacent the at least one recess, the surface of the semiconductor device structure and a surface of the first material layer in the at least one recess being located in substantially the same plane following planarizing.

22. (Previously presented) The method of claim 20, wherein planarizing comprises substantially concurrently etching the first material layer and the stress buffer material at substantially the same rate so as to expose the surface of the semiconductor device structure adjacent the at least one recess with the surface of the semiconductor device structure and a surface of the first material layer in the at least one recess being located in substantially the same plane following planarizing.